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PERSONAL AUTHOR(S)
O. P. Vu, Milt Boden, and Paul M. Zavracky

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18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
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. ABSTRACT (Continue on reverse if necessary and identify by block number)

This report documents the findings of Kopin Corporation during the first five months of the program. Significant results include the development of a new process sequence, and a verification of the low stress in ZMR (ISE) material. Current direction is aimed at the fabrication of both accelerometers and pressure sensors using our advanced SOI process.

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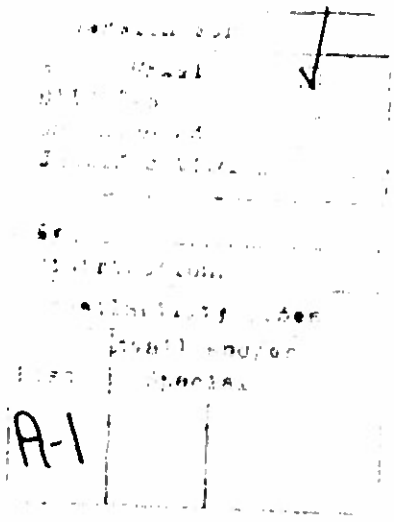

INTERIM REPORT

(Oct -Feb)

SMART MICROSENSORS FOR HIGH TEMPERATURE APPLICATIONS

Contract # DAALO3-90-C-0029

Contracting Officer: Patsy S. Ashe

by D.P. Vu, Milt Boden,
Rick Morrison, and P. M. Zavracky

Kopin Corporation
695 Myles Standish Blvd.
Taunton, Massachusetts 02780

TABLE OF CONTENTS

LIST OF FIGURES

TECHNICAL OBJECTIVES FOR THIS REPORTING PERIOD:

Task 1: Diaphragm Design

In this first reporting period significant progress has been made toward achievement of the goals of this contract. We re-examined the results on diaphragms obtained during phase I to determine the best starting point for the phase II program. Results of this examination are reported and indicate a thickness variation in the silicon layer in the direction of the ZMR scan. We therefore have established a unique process sequence which we believe will totally alleviate any thickness non-uniformity issues.

A mask set has been designed and fabricated which facilitates the improved fabrication sequence.

Further testing by an independent consultant verifies extremely low stress in our ISE layers. These results support our believe that ISE SOI will have a significatn impact the state-of-the-art in microsensor manufacturing.

Preliminary Process tests suggest our approach will be very rewarding.

Task 2: Circuit Design

A literature search has begun resulting in several important references.

Task 5: Modeling

No progress to report in this area.

RESULTS:

Diaphragm Design

During this reporting period, wafers from Phase I which had been processed were closely examined. Photographs such as those shown in figures 1a and 1b indicate very exciting results. The Nomarski micrograph of figure 1a shows a series of bridge structures of increasing length at the top and to the right of the photo and shows a series of cantilever structures at the bottom and to the left side of the photograph. It is very clear from this picture that the bridges are all freely suspended. The photo can be interpreted in the following way. The depth of field of the microscope is limited to about two microns or less at this magnification(400x). The structures being observed were fabricated on a 3 micron oxide layer and had 1 micron of silicon film thickness. Therefore, from the base of the beam or bridge to its free area there exists a step height of 3 micron. If the microscope is focussed on the free region of the bridge, as in the photo, then the bridge bases will be out of focus. This fact is readily apparent in the photograph. If the free region of the beam had collapsed onto the substrate, then it would be out of focus in the photograph. None of the bridge structures are out of focus in the figure 1a indicating that they are all freely supported 3 microns above the substrate. The cantilever structures did not fair as well. Only two of those visible in the photograph are actually in focus, indicating that most of the cantilevers have indeed collapsed onto the substrate. These results are excellent and exhibit the tremendous potential of this technology. The longest bridge shown in the photograph is about 200 microns in length and 10 microns wide. During Phase I we demonstrated diaphragms 600 microns across. Diaphragms as large as these are difficult to manufacture in polysilicon because of built in stresses. ISE material has very low stress and is therefore an ideal material for sensor applications.

Photographs such as that shown in figure 1b were taken with the SEM and indicate cantilever beams with apparently good thickness uniformity. However, in examining wafers after the ZMR process but prior to defining the ISE structures and etching the oxide we became aware of an new phenomena. Figure 2a shows a brightfield micrograph of such a wafer. A very faint optical interference pattern is observed. Close examination indicates that the pattern seems to intensify around the etched holes in the oxide layer. These are the features that readily apparent in the photograph. This slight interference pattern could be an indication of thickness non-uniformity in the ISE layer. Figure 1b shows a similar wafer after the poly resist has been patterned. This pattern defines the areas were the silicon epitaxial layer will remain after etching. In this photograph, the interference pattern is much more pronounced. It is also worth noting that the larger the hole in the oxide, the greater the number of fringes surrounding it.

In order to examine this phenomena more closely, we cross sections samples of the material shown in figure 2a. The results are shown in figure 3. This sample was cross-sectioned in a Philtec. This machine employs a 1" spindle upon which the abrasive compound is applied. The sample is mounted in a simple holder and brought into contact with the rotating spindle. This action creates a cylindrical grove in the sample. In figure 1a, the groove can be clearly seen, traversing the photograph at 45^{0}. Because the holes in the oxide are relatively small, many have been intersected by the groove. At the center of the groove, the silicon substrate has been reached and appears as a band about 1.5 cm wide in the photograph. The closely spaced parallel features that are oriented at right angles to the center band (and therefore the groove) are microgrooves that are an artifact of the spinning abrasive cylinder used to

a)

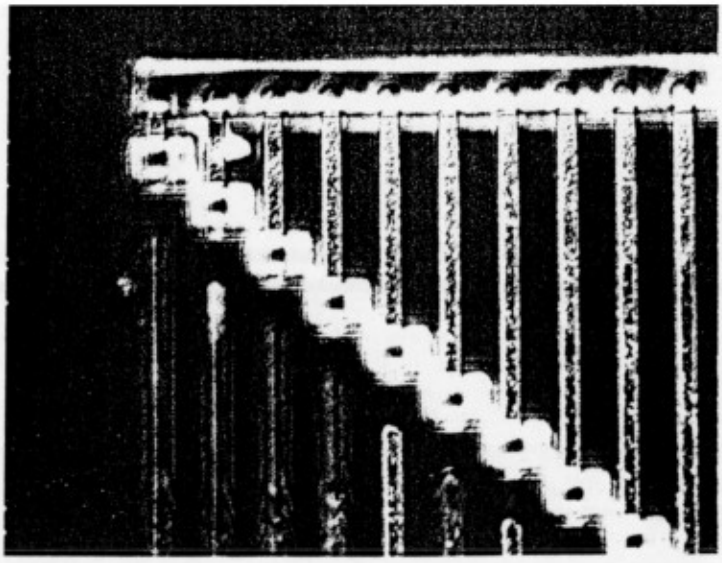

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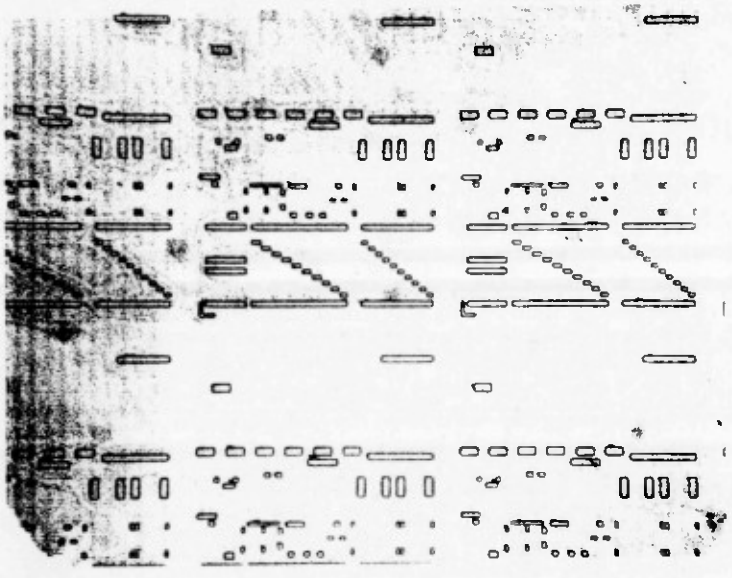
Figure 1. Micromechanical structures created during Phase I of this program. a) Nomarski photograph of cantilever beams and bridges fabricated in ISE SOI. b) SEM micrograph of a free cantilever.

a)



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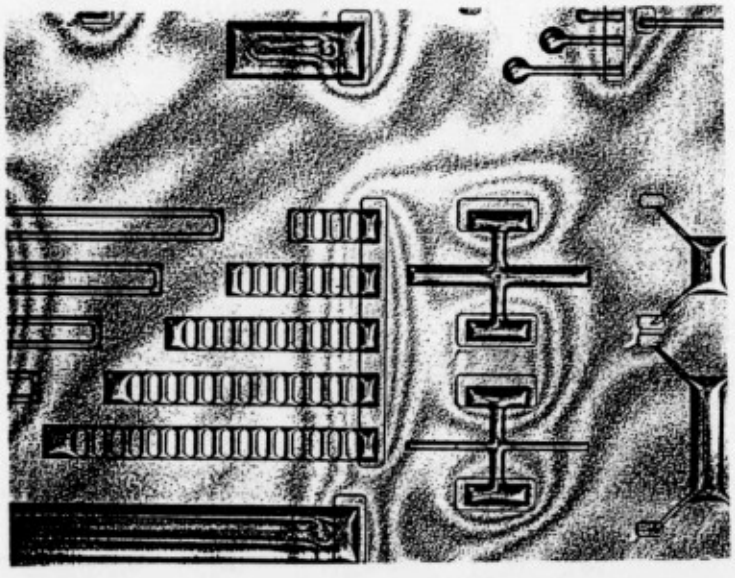


Figure 2. Photographs showing fringes after the ZMR process. a) Brightfield micrograph of an ISE SOI wafer in which the oxide was patterned to define openings in the silicon oxide through which the microstructures will contact the substrate. b) A Nomarski micrograph of the wafer after the photoresist has been applied and patterned.

create the groove. Ignore the patterned features for the moment. On either side of the center band are two nearly identical bands which contain widely spaced interference patterns. These bands represent the silicon oxide isolation layer in the SOI material. This is the oxide that was etched to permit the epitaxial silicon to come into contact with the silicon substrate. Two bands are observed because a cylindrical groove was ground into the sample. Each layer that as been completely ground through will display two symmetric bands in the photograph. A second pair of layers are observed on the outlining sides of the oxide bands. These are the epitaxial silicon bands. The interface between the silicon oxide and the silicon epitaxy is very smooth and straight. The same can not be said for the epitaxial silicon surface. Within the silicon layer, a much tighter set of optical interference fringes is observed. The index of refraction of silicon is about 3.85 at visible wavelengths whereas the index for silicon oxide is only 1.45. This difference accounts for some of the spacing difference observed. This photograph was take under green light illumination at a wavelength of approximately 0.5 microns. A fringe dark fringe will appear every half wavelength of silicon thickness or about every 0.5/2/3.85 = 0.066 microns. In a thin silicon area, thirteen fringes appear indicating that the silicon thickness there is about 0.85 microns. In the thicker areas, perhaps as many as 20 fringes may be counted. The corresponding silicon thickness would be about 1.32 microns (The fringes are easier to count in figure 3b). The greatest silicon thickness variation is observed around the large oxide etch feature that appears along the diagonal of the photograph. Figure 1b shows a close-up of this feature.

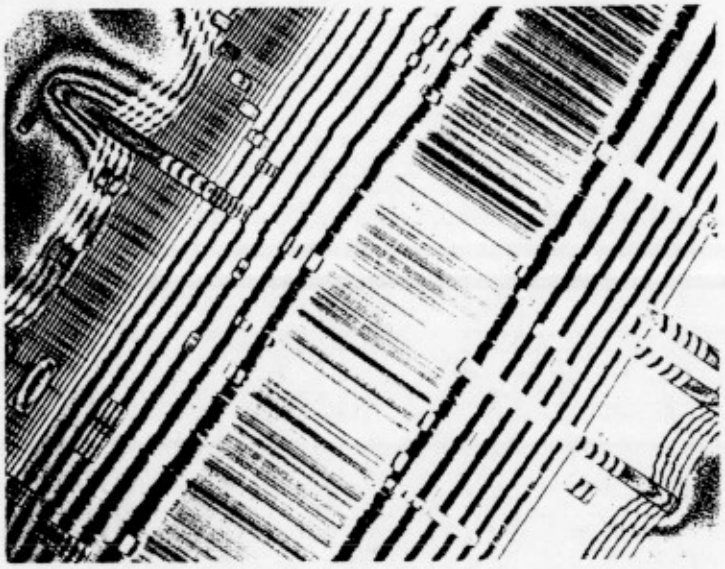
Above the silicon layer, another set of parallel fringes is observed. These have about the same spacing as the oxide layer, and indeed are a result of the capping oxide. The surface of this oxide layer is the uppermost surface of the sample and so, the outside edge of the grove corresponds to the top most fringe of this upper oxide layer. Beyond these fringes, the unaltered surface of the sample is visible. Again, fringes can be observed throughout this area. These fringes are now confirmed to arise from the silicon layer.

Since the groove is cylindrical and not v-shaped, the angle of the cross-section is gradually decreasing to zero at the center of the groove. The variation in this angle from the center to the edge of the groove accounts for the non-uniform spacing of the fringes within a particular layer.

In figure 3b, we see that the largest oxide etch feature contains two sets of fringes. The top most fringes which appear to be uniformly space, are due to the capping layer. Below this is the epitaxial silicon which inside this feature comes into contact with the silicon substrate surface because the oxide has been etched away. Counting the fringes within the silicon layer may be difficult, but results in a count of about 20. Therefore, the silicon thickness inside the oxide cut is the same as that immediately surrounding it.

The observed silicon thickness variation appears to be due to the disturbance of the ZMR process by the abrupt change in the composition of the substrate at the oxide cuts. The lack of oxide in these regions certainly affects the temperature of the melt front. The effect may be countered or at least minimized by reducing the thickness of the silicon oxide. This choice is undesirable because it makes the recrystallization process more difficult to control and it lowers the yield for free structures as determined in Phase I. A second approach might be to increase the thickness of the capping layer. This approach is also undesirable in that it requires more process time, and therefore results in higher cost. After careful consideration, we decided to explore other paths.

a)



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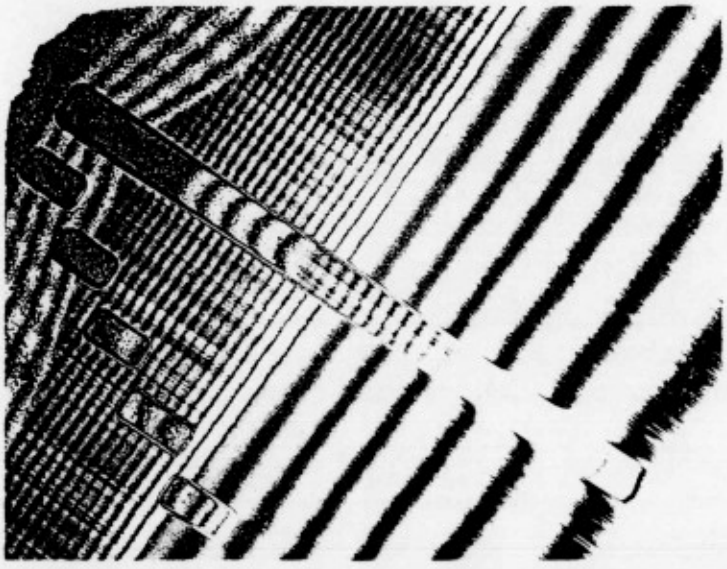


Figure 3. Cross-sections of patterned wafers.

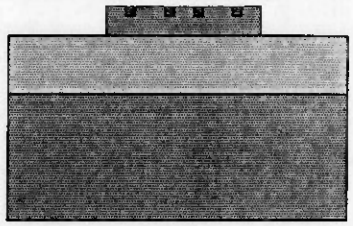
Our basic concept is depicted in figure 4. To totally avoid the thickness uniformity problem just described, our new process begins with a standard ISE SOI wafer. Starting with a standard SOI wafer has advantages in itself. It frees the sensor manufacturer from having to run the ISE process at his facility, and therefore increases the number companies that could use the process developed under this contract. It also avoids the problem of wafer distortion that occurs during the recrystallization process. This distortion limits the minimum feature size possible, due to alignment problems. Continuing with the process, the ISE epitaxial silicon layer is first patterned to define the diaphragm area. As a result of this process, the underlying oxide is exposed in those areas were the silicon epi has been removed. The oxide can then be etched. This process may be performed wet, as it is required that the diaphragms be undercut to some extent. The precision of the undercut is dependent on the size of the diaphragm required. Polysilicon is deposited next and is expected to totally surround the edge of the diaphragm as shown in the figure. The oxide must be removed to free the diaphragm. This aspect of our process will be discussed in greater detail in the next few paragraphs.

The most important and critical aspect of this new process, is that the polysilicon layer actually surround and adhere to the epitaxial silicon diaphragm. Before committing to this approach, Kopin prepared some samples using the mask set from Phase I. In figure 5, a photograph of a test sample is shown. This photo was obtained by cleaving a sample such that the cleave intersected the diaphragm. A slight oxide etch was performed to enhance the contrast between the poly, oxide and epitaxial layers, and the sample was prepared for the SEM. Figure 5b shows our interpretation of the SEM photograph. The oxide layer has been clearly delineated. It is about 3 microns thick. While it is difficult to see, the single crystal silicon diaphragm layer protrudes out over the edge of the oxide region indicating the extent of the undercut during the oxide etch. The polysilicon, which looks somewhat lighter than the epitaxial silicon in the picture has surrounded the protruding epitaxial layer and is conformal with the oxide layer. This result indicates that the use of polysilicon as a clamp is well justified.

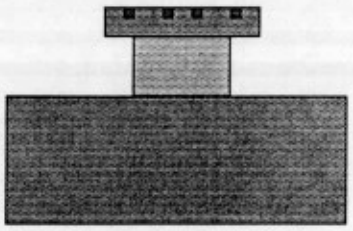
To understand in more detail the process for etching the oxide out from beneath the diaphragm we have created the illustration shown in figure 6. After the epitaxial diaphragm has been defined, it will be reoxidized slightly. This oxide will be etched to create anchor points in the top of the diaphragm. These are places were the subsequent polysilicon deposition will come directly in contact with the epitaxial silicon. We call them anchors because they will be used to support the diaphragm during subsequent processing. After the poly has been deposited, it can be patterned, and the oxide on the epitaxial diaphragm can be used as a stop to prevent the diaphragm from being etched during the poly etch process. With the poly supports defined, the wafer will be emersed in a concentrated HF bath. The HF will etch the thin oxide between the poly support and the epitaxial silicon. The etching will continue around the edge of the protruding portion of the diaphragm and finally into the underlying oxide. With enough time in the bath (2hr), the HF will completely remove the oxide from beneath the diaphragm. At this point, the diaphragm is supported by the anchor points. To reseal the diaphragm, the wafer is oxidized. Oxide forms on the poly support and the epitaxial layer and eventually the oxide layers will contact to seal the diaphragm. If the oxidizing ambient were pure oxygen, then the oxidation process would continue under the sealed diaphragm until all the oxide was consumed. This would create a vacuum inside the sealed cavity. The sensor made using this process would be an absolute pressure sensor. Different ambients could be used during oxidation. For instance, argon could be added. The final pressure inside the sealed cavity would depend on the percentage of argon in the oxidizing ambient.

1) Implant p- and p+ regions and activate.

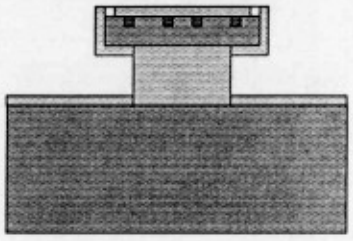
2) Pattern and etch silicon epi layer.



3) Etch underlying oxide layer.

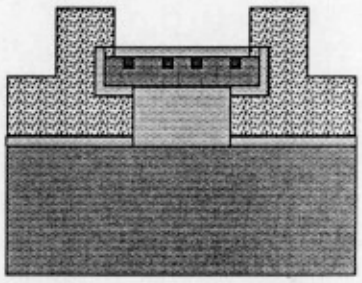


4) Reoxidize the wafer and pattern oxide for poly anchors.



5) Deposit and pattern polysilicon. The polysilicon will be used to support the silicon diaphragm.

6) Etch thin oxide and underlying oxide in concentrated FH.



7) Reseal Diaphragm by oxidizing the silicon diaphragm and poly silicon support.

8) Thin Metal + Shield.

9) Thick Metal Deposition and Pattern.

10) Oxide Etch.

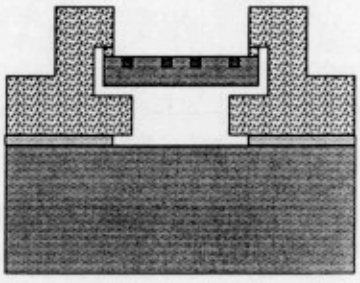
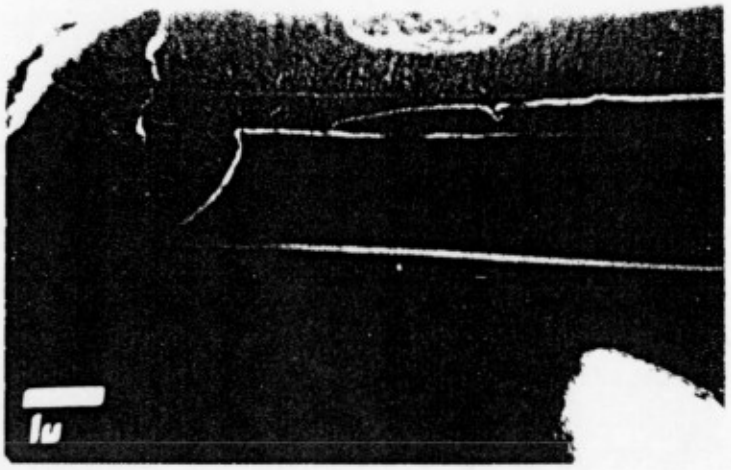


Figure 4. Basic Sensor Process

a)



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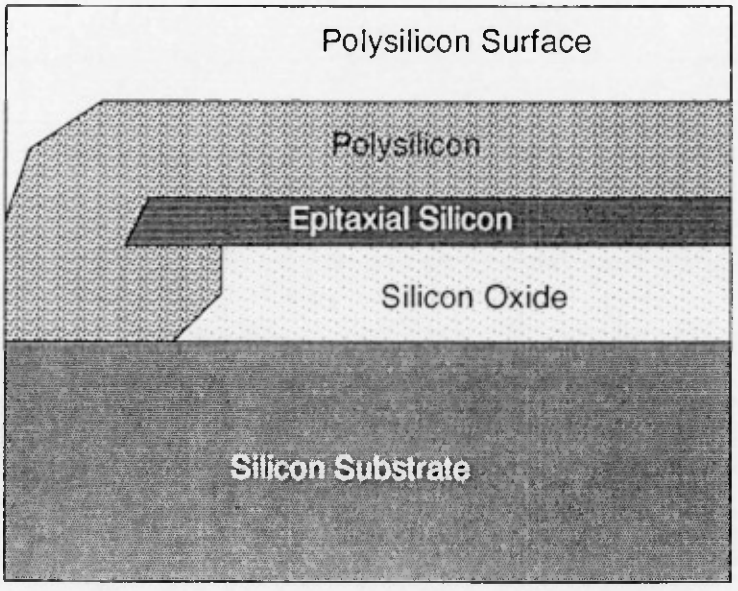


Figure 5. a) SEM photograph of the polysilicon step coverage at the edge of the diaphragm. b) Drawing showing our interpretation of the SEM information.

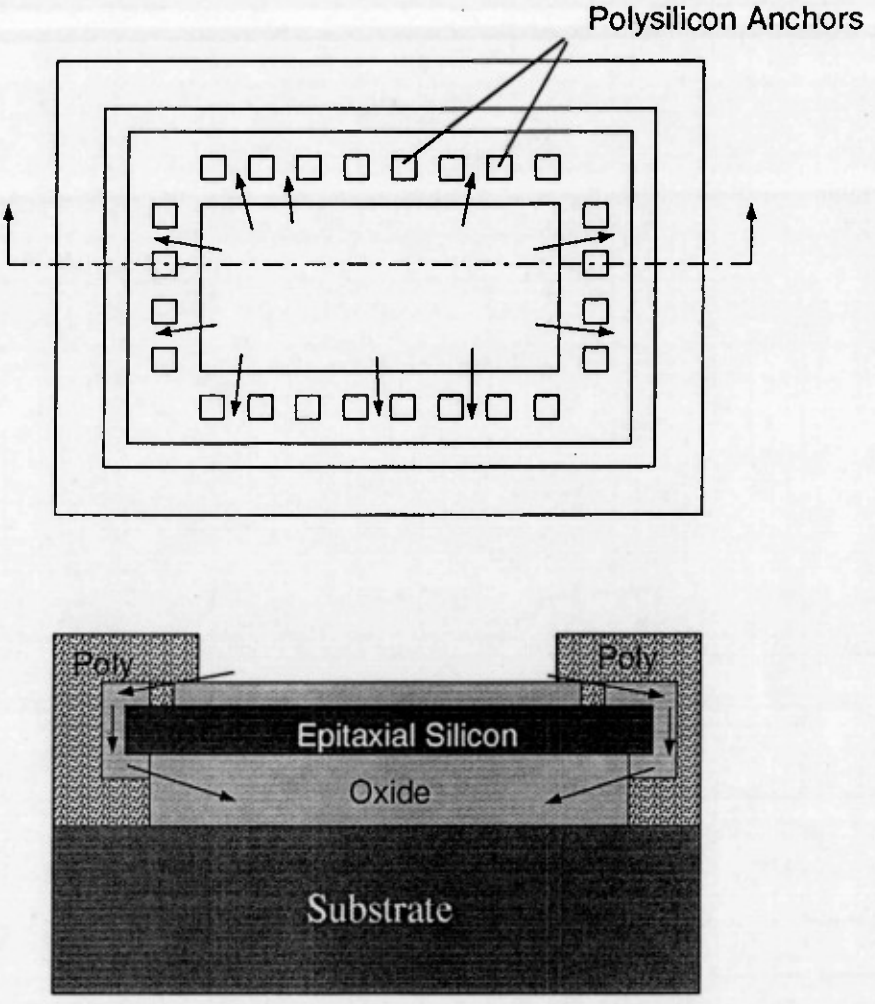


Figure 6. Detail of oxide undercut process. The arrows show the path of the HF etchant.

We have also considered a process in which the wafer is back etched to allow access to the backside of the diaphragm. The result of this process is depicted in figure 7.

Process specifications for the above sensor were developed during this quarter. These are presented in Appendix A and B of this document. The complete process requires the addition of piezoresistor implantation and metallization to contact the resistors. The process steps are included in our specifications.

A mask set has been designed, review and manufactured for this program. While the specific objectives of this contract call out the development of both capacitive and piezoresistive pressure sensors, the process describe above could be used as well for accelerometers. We therefore generated a mask set which includes both structures. Figure 8 shows a few characteristic structures that can be found in our mask design. The mask set includes diaphragms ranging from 100x150 microns, 300x350 microns, 700x750 microns, and 1x1.5mm.

We employed the services of Professor Henry Guckel at the University of Wisconsin, a world renowned expert on silicon microsensors, used his special measurement capabilities to determine the magnitude of the mechanical stresses in our ISE wafers. A letter recently sent to me is attached in appendix C. In figure 9, SEM micrographs show some of the cantilever structures created by Henry's group. The importance of Henry's results can not be over emphasized. In order to make good micromechanical structures, stress free materials are required. As he reports in his letter, "the enclosed SEM's show the results and yield the conclusion that the film is not only strain free but that there is virtually no interface strain." With results like these and our own successes, we can be very confident about the success of this program, and the important impact it will have on the sensor community.

Circuit Design

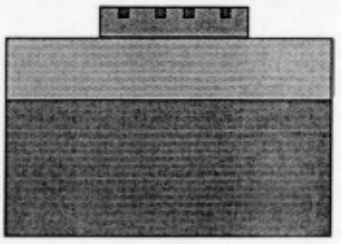
A literature search has begun and is continuing. I have include several references that contain appropriate information or circuit designs that we will analyze and consider for our application. As more literature becomes available, I will continue to reference the relevant papers.

Modeling

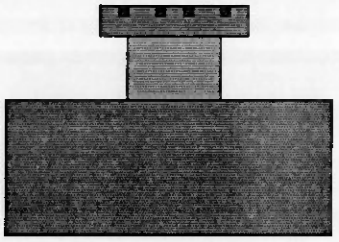
During the first several months of this program, our proposal calls for the initiation of a modeling effort. This scheduling is inappropriate in that a definition of the structure is required before specific aspects can be modeled. During the next several months, Kopin will begin to focus its resources in this area. As specified in our proposal, our objectives are to develop models to predict the mechanical properties of the sensors and to use SPICE to evaluate circuit designs.

1) Implant p- and p+ regions and activate.

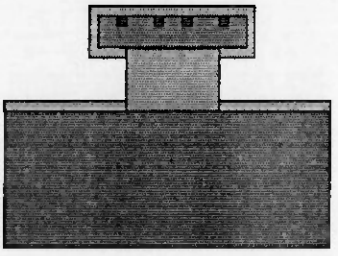
2) Pattern and etch silicon epi layer.



3) Etch underlying oxide layer.



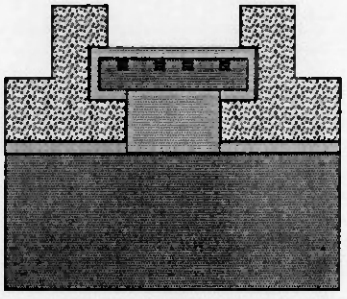
4) Reoxidize the wafer.



5) Deposit and pattern polysilicon. The polysilicon will be used to support the silicon diaphragm.

6) Nitride Dep (LPCVD)

7) Backlap wafer to 5 mils.



8) Back-etch(KOH) silicon wafer.

9) Thin Metal + Shield.

10) Thick Metal Deposition and Pattern.

11) Oxide Etch.

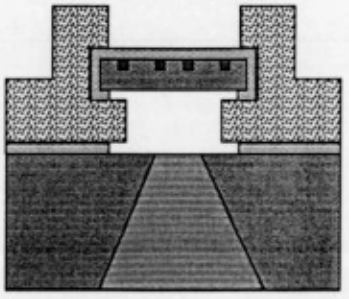


Figure 7. Back etched SOI pressure sensor process.

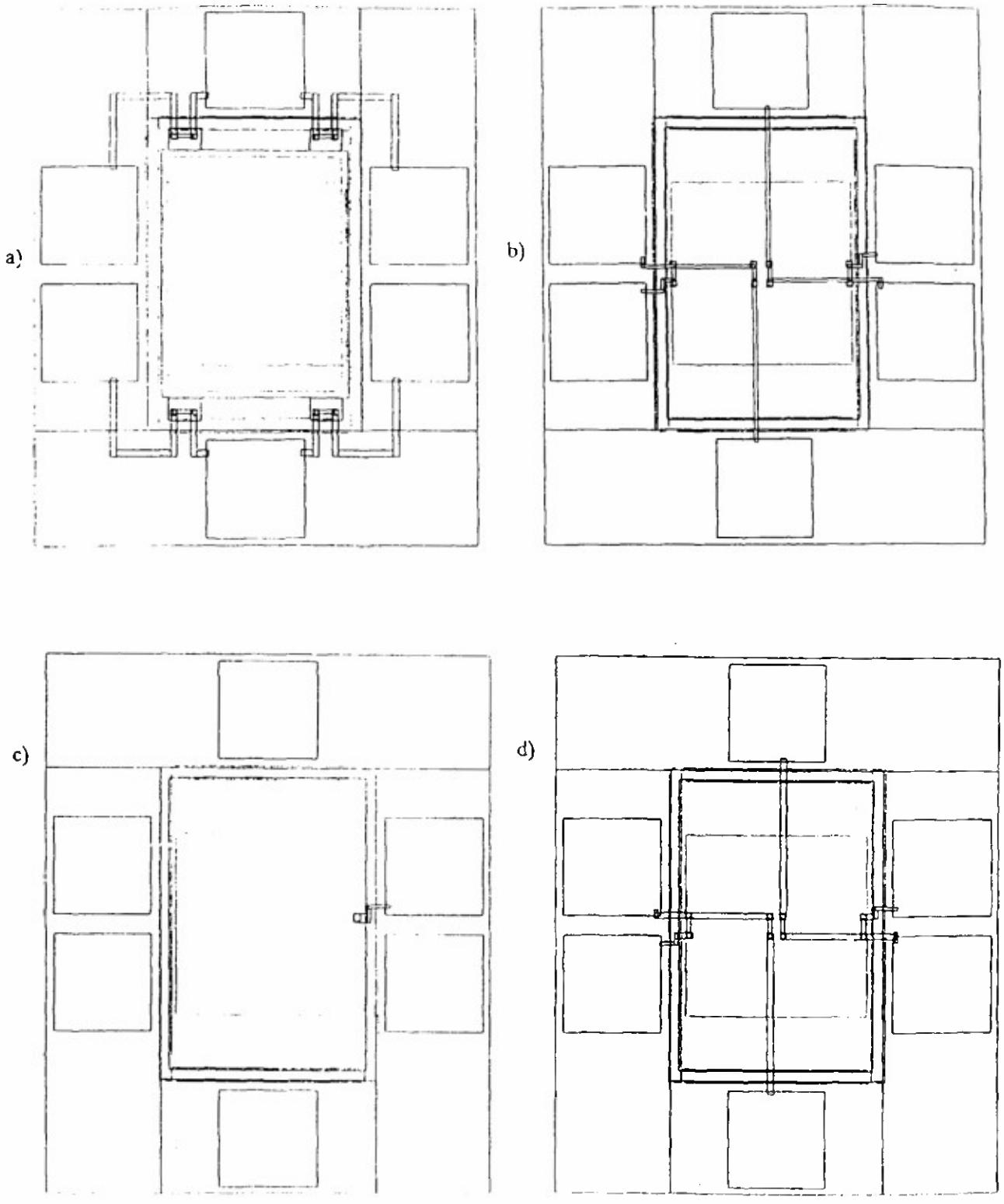
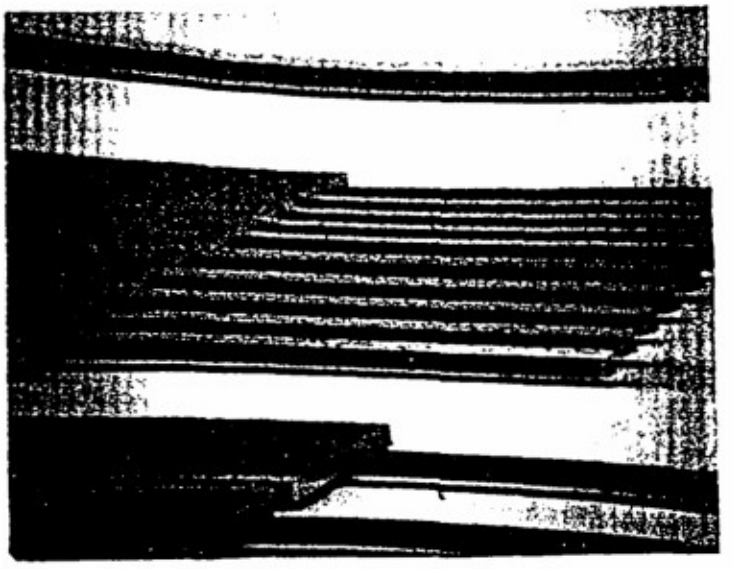


Figure 8. Some structures appearing on our sensor mask set. a) Accelerometer b) Piezoresistive Pressure Sensor c) Capacitive Pressure Sensor d) Pressure sensor similar to b)

a)



b)

Figure 9 SEM micrographs of cantilever structures produced at the University of Wisconsin

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APPENDIX A

TOP ETCHED ISE SENSOR PROCESS SPECIFICATION

PRESSURE SENSOR (back side etch) Sensor Test Mask Lot no. _____

PROCESS STATION	DESCRIPTION	QTY	OP	DATE	CHECK	COMMENTS
	Wafer start	ZMR wafer 3 in, 8 - 10 mil				Substrate no. _____ _____ _____ _____
						Si thickness _____ _____ _____ _____
	Initial Oxide	Clean				
		H2SO4:H2O2, 20 min				
		30:1 HF dip, 30 sec				
		Megasonic 15 min				
		QDR SRD				
		Oxidize 510, 32 min				
		Measure				Mean _____ Range _____
	Alignment PR	HMDS				
		Coat front				
		Bake				
		Coat back				
		Expose, Front and Back				
		Develop				
		Bake				
	Alignment Etch	Etch oxide				
		Etch Silicon				
		Strip Resist				
	P+ PR	HMDS				
		coat				
		align				
		develop				
		bake (120 deg C, 10 min.)				
		inspect				
	P+ implant	etch oxide BOE				
		bake				
		implant				Dose 1E15_____ Energy 30 keV_____ Boron_____
		resist strip (LFE + wet)				
	Resistor PR	HMDS				
		coat				
		align				
		develop				
		bake (120 deg C, 10 min.)				
		inspect				
	Resistor implant	implant				Dose 2.2E13_____ Energy 30 keV_____ Boron_____
		resist strip (LFE + wet)				
	Oxide 1 PR	HMDS				
		coat				
		align				
		develop				
		bake (120 deg C, 10 min.)				
		inspect				
	Oxide Etch	etch				
		resist strip				
		post inspect				
	Diaphragm PR	HMDS				
		coat				
		align				
		develop				
		bake (120 deg C, 10 min.)				
		inspect				

ROCESS CATION	DESCRIPTION	QTY	OP	DATE	CHECK	COMMENTS
	Diaphragm Etch	Etch ISE (HNO3:HF:H2O) (50: 3: 20)				
		Etch IO (BOE)				
		Strip Resist				
	Poly Dep	Clean				
		H2SO4:H2O2 20 min				
		30:1 HF:H2O 30 sec				
		Megasonic 15 min				
		QDR SRD				
		Deposite				
		Measure				
	Poly PR	HMDS				
		Coat				
		align				
		develop				
		bake (120 deg C, 10 min.)				
		inspect				
	Poly Etch	Etch (HNO3:HF:H2O)				
		Resist Strip				
	Barrier oxide	Clean				
		H2SO4:H2O2 20 min				
		30:1 HF dip 30 sec				
		Megasonic 15 min				
		Oxidation				
		Measure				
	TEOS dep	TEOS deposition				
		measure				
	N2 anneal	anneal				tube no. _____ recipie _____
		inspect				
	TEOS dep	TEOS deposition				
		measure				
	N2 anneal	anneal				tube no. _____ recipie _____
		inspect				
	Backside PR	HMDS				
		coat				
		align				
		develop				
		bake (120 deg C, 10 min.)				
		inspect				
	Backside etch	Etch oxide (BOE)				
		Resist Strip				
		Silicon Etch KOH				
		Oxide etch BOE				

Pressure Sensor (back side etch) Lot no. _____ Page 3

PROCESS STATION	DESCRIPTION	QTY	OP	DATE	CHECK	COMMENTS
	Dielectric Oxide	Clean				
		H2SO4:H2O2 20 min				
		30:1 HF 30 sec				
		Megasonic 15 min				
		Oxidation				
		Measure				
	Contact PR	HMDS				
		coat				
		align				
		develop				
		inspect				
		bake				
	Contact etch	etch (BOE1)				time _____
		resits strip				
	Metal dep	clean (megasonic)				
		dep				
	Metal PR	coat				
		align				
		develop				
		inspect				
		bake (10 min, 120 C)				
	Metal etch	etch				
		resist strip				
	Sinter					
	Bond metal PR	HMDS				
		coat (Image reversal)				
		align				
		develop				
		inspect				
		bake				
	Bond metal dep	deposition				
	Liftoff	liftoff				
		inspect				

APPENDIX B

BACK ETCHED ISE SENSOR PROCESS SPECIFICATION

PRESSURE SENSOR (top etch) Sensor Test Mask Lot no. _____

PROCESS STATION	DESCRIPTION	QTY	OP	DATE	CHECK	COMMENTS
	Wafer start	ZMR wafer 3 in, 25 mil				Substrate no. _____ _____ _____ _____
						Si thickness _____ _____ _____ _____
	Initial Oxide	Clean				
		H2SO4:H2O2, 20 min				
		30:1 HF dip, 30 sec				
		Megasonic 15 min				
		QDR SRD				
		Oxidize 510, 32 min				Tube_____ Boat_____
		Measure				Maan _____ Range _____
	P+ PR	HMDS				
		coat				
		align				
		develop				
		bake (120 deg C, 10 min.)				
		inspect				
	P+ implant	etch oxide				
		implant				Dose 1E15_____ Energy 30 keV_____ Boron _____
		resist strip (LFE + wet)				
	Resistor PR	HMDS				
		coat				
		align				
		develop				
		bake (120 deg C, 10 min.)				
		inspect				
	Resistor implant	implant				Dose 2.2E13_____ Energy 30 keV_____ Boron _____
		resist strip (LFE + wet)				
	Diaphragm PR	HMDS				
		coat				
		align				
		develop				
		bake (120 deg C, 10 min.)				
		inspect				
	Diaphragm Etch	Etch ISE (HNO3:HF:H2O)				
		(50 : 3 : 20)				
		Etch IO (BOE)				
		Strip Resist				
	Cover oxide	Clean				
		H2SO4 H2O2 20 min				
		30 1 HF dip 30 sec				
		Megasonic 15 min				
		QDR SRD				
		Oxidation (partial steam)				Target 0.25 microns Tube _____ Boat _____
		Measure				

PROCESS STATION	DESCRIPTION	QTY	OP	DATE	CHECK	COMMENTS
	Anchor PR	HMDS				
		Coat				
		align				
		develop				
		bake (120 deg C, 10 min.)				
		inspect				
	Anchor Etch	Etch BOE				
		Resist Strip				
	Poly Dep	Clean				
		H2SO4:H2O2 20 min				
		30:1 HF:H2O 30 sec				
		Megasonic 15 min				
		QDR SRD				
		Deposite				
		Measure				
	Poly PR	HMDS				
		Coat				
		align				
		develop				
		bake (120 deg C, 10 min.)				
		inspect				
	Poly Etch	Etch (HNO3:HF:H2O)				
		Resist Strip				
	Undercut Etch	Etch Concentrated HF				
		Special Rinse & Dry				
	Sealing Oxide	Clean H2SO4:H2O2				
		30:1 HF				
		QDR				
		SPIN DRY ONLY				
		Oxidation				
		Measure				
	Contact PR	HMDS				
		coat				
		align				
		develop				
		inspect				
		bake				
	Contact etch	etch BOE				time _____
		resits strip				

PROCESS STATION	DESCRIPTION	QTY	OP	DATE	CHECK	COMMENTS
	Metal dep	clean (megasonic)				
		dep				
	Metal PR	coat				
		align				
		develop				
		inspect				
		bake (10 min, 120 C)				
	Metal etch	etch				
		resist strip				
	Sinter					
	Bond metal PR	HMDS				
		coat (Image reversal)				
		align				
		develop				
		inspect				
		bake				
	Bond metal dep	deposition				
	Liftoff	liftoff				
		inspect				

APPENDIX C

LETTER FROM PROF. H. GUCKEL
UNIVERSITY OF WISCONSIN, MADISON

Department of Electrical and Computer Engineering

University of Wisconsin-Madison

1415 Johnson Drive
Madison, WI 53706-1691
FAX 608 / 262-1267

Dr. Paul M. Zavracky
Kopin Corporation
695 Myles Standish Boulevaro
Taunton, MA 02780

Dear Paul:

This letter is prompted by our recent telephone conversation and is sort of a short summary of the SOI work which has been started here.

The work is staffed by a new student, Mr. Lee, who is quite good and does of course have access to the skills of the other students in our group.

The initial work has concentrated on understanding the 2 micron thick layers and on process design for the 20 micron thick SOI.

The 2 micron thick material has been improved a lot over the earlier versions which were tested here by Jeff Sniegowski, whose services were never billed to Kopin. The new film is essentially strain free. This statement applies to strain levels above 10^8 dyne/cm^2. The evidence for this is found in our ability to make 10 micron wide cantilevers of nearly arbitrary lengths and of course the absence of buckling in either compressive or tensile strain test structures.

The surface adhesion problem after HF etching is present and severe because the mating surfaces are very smooth. We have avoided this by using sublimation techniques and silicon nitride passivation. The enclosed SEM's show the results and yield the conclusion that the film is not only strain free but that there is virtually no interface strain. I am somewhat envious of these results, because this is not true for polysilicon and metal films. The interface is always strained; and therefore, the average strain in the film is a

function of thickness. The conclusions are therefore very good and I do believe that you can claim films which are strain free and without interface strain at any film thickness. This statement must be restricted: it applies to the films which we have seen and there may be a dependence on doping level and distribution.

The mechanical characterization is now at the point of measuring Young's modulus. This will be done by using resonant beams along the 110 direction. I do not expect any surprises and anticipate a somewhat higher Young's modulus than in polysilicon. This may also be true for the Q. Measurements will start in about 3 weeks and are based on a four mask sequence.

A third set of experiments is also in progress. The effect of doping on strain must be known because this influences sensor design. This is related to the fact that junctions in polysilicon are not very good, and we know that they are acceptable in SOI films.

In the sensor application area we have made some progress. The questions of what is the advantage of SOI only, and how is it combined with polysilicon and LIGA processing are our basis. I am absolutely convinced that the 20 micron material can be used to make the world's most sensitive accelerometer. But the proof is in a fabricated device.

The work is generating a very nice masters report. This will be submitted to you but we will also keep you informed of current progress.

Best Personal Regards,

Henry Guckel
Professor